PRODUCT/PROCESS
CHANGE NOTIFICATION

PCN AMS/15/9514

Analog, MEMS and Sensors Group

New material set in ST Bouskoura for AMS products in SO8 and SO14 packages

WHAT:

Progressing on the activities related to quality continuous improvement, ST is glad to announce a new material set for AMS products in SO8 and SO14 packages produced in ST Bouskoura.
Please find more information related to material change in the table here below.

Material	Current process	Modified process	Comment
Diffusion location	ST Ang Mo Kio (Singapore)/ UMC	ST Ang Mo Kio (Singapore)/ UMC	No change
Assembly location	ST Bouskoura	ST Bouskoura	No change
Molding compound	Sumitomo G700K / Sumitomo G630AY	Sumitomo G700KC	To solve some sporadic delamination on lead issues sawn in production. Move to High reliability compound
Die attach	Ablestick 8601-S25	Ablestick 8601-S25	No change
Leadframe	Copper preplated NiPdAgAu Copper preplated ag spot	Copper preplated ag spot	No change
Wire	Copper 1 mil	Copper 1 mil	No change
Plating	NiPdAgAu Sn	Sn	No change

Samples of vehicle test are available now and other samples will be launched upon customer's request. Please submit requests for samples within 30 days of this notification.

WHY:

This material change will contribute to ST's continuous quality product improvement and ensure a consistent assembly process through all the SO production lines.

HOW:

The qualification program consists mainly of comparative electrical characterization and reliability tests.

You will find here after the qualification test plan which summarizes the various test methods and conditions that ST uses for this qualification program.

WHEN:

The new material set will be implemented for AMS products in Q1/2016 in Bouskoura.

Marking and traceability:

Unless otherwise stated by customer's specific requirement, the traceability of the parts assembled with the new material set will be ensured by new internal sales type, date code and lot number.

The changes here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all the information reported on the relevant datasheets.
There is -as well- no change in the packing process or in the standard delivery quantities.

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change. After acknowledgement, lack of additional response within the 90 day period will constitute acceptance of the change (Jedec Standard No. 46-C).
Shipments may start earlier with the customer's written agreement.

Reliability Report

New Halogen free material set for SO in ST Bouskoura

General Information	
Product Line	*0393, 0339, 0084*
Product Description	Dual comparator bipolar, Quad comparator bipolar, quad Jfetl op amp
P/N	*LM2903YDT, LM2901YDT, TL084IYDT*
Product Group	*AMS*
Product division	*VMA*
Package	*SO8/14*
Silicon Process technology	*Bipolar,Jfet*

Locations	
Wafer fab	*ST Singapore,*
Assembly plant	*ST Bouskoura (Morocco)*
Reliability Lab	*ST Grenoble, ST Bouskoura*

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	Stress test qualification for automotive grade integrated circuits
AEC-Q101	Stress test qualification for automotive grade discrete semiconductors
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

To qualify a new molding compound for SO package in Bouskoura (Sumitomo G700KC which is an evolution of Sumitomo G700K already in use in Bouskoura) for AMS (Analog Mems & Sensor) group.

3.2 Conclusion

Qualification Plan requirements have been defined and today partially achieved. It is stressed that reliability tests have to show that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests have to demonstrate the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

LM2903YDT

life.augmented

LM2903

Low-power dual voltage comparator

Datasheet - production data

N
DIP8
(plastic package)

D
SO8
(plastic micropackage)

P
TSSOP8
(thin shrink small outline package)

S
MiniSO8
(plastic micropackage)

DFN8 2x2 mm
(plastic micropackage)

Features

- Wide single supply voltage range or dual supplies +2 V to +36 V or ±1 V to ±18 V
- Very low supply current (0.4 mA) independent of supply voltage (1 mW/comparator at +5 V)
- Low input bias current: 25 nA typ.
- Low input offset current: ±5 nA typ.
- Input common-mode voltage range includes negative rail
- Low output saturation voltage: 250 mV typ. (I_O = 4 mA)
- Differential input voltage range equal to the supply voltage
- TTL, DTL, ECL, MOS, CMOS compatible outputs
- Automotive qualification

Related products

- See LM2903W for similar device with higher ESD performances
- See LM2903H for similar device with operating temperature up to 150 °C

Description

This device consists of two independent low-power voltage comparators designed specifically to operate from a single supply over a wide range of voltages. Operation from split power supplies is also possible.

In addition, the device has a unique characteristic in that the input common-mode voltage range includes the negative rail even though operated from a single power supply voltage.

LM2901YDT,

LM2901

Low-power quad voltage comparator

Features

- Wide single supply voltage range or dual supplies for all devices: +2 V to +36 V or ±1 V to ±18 V
- Very low supply current (1.1 mA) independent of supply voltage (1.4 mW/comparator at +5 V)
- Low input bias current: 25 nA typ.
- Low input offset current: ±5 nA typ.
- Input common-mode voltage range includes negative rail
- Low output saturation voltage: 250 mV typ. (I_O = 4 mA)
- Differential input voltage range equal to the supply voltage
- TTL, DTL, ECL, MOS, CMOS compatible outputs

N
DIP14
(Plastic package)

D
SO-14
(Plastic micropackage)

P
TSSOP14
(Thin shrink small outline package)

Q4
QFN16 3x3
(Plastic micropackage)

Description

This device consists of four independent precision voltage comparators, which are designed specifically to operate from a single supply over a wide range of voltages. Operation from split power supplies is also possible.

These comparators also have a unique characteristic in that the input common-mode voltage range includes the negative rail even though operated from a single power supply voltage.

***TL084IYDT*:**

TL084, TL084A, TL084B

General purpose JFET quad operational amplifiers

Datasheet — production data

Features

- Wide common-mode (up to V_{CC}^{+}) and differential voltage range
- Low input bias and offset current
- Output short-circuit protection
- High input impedance JFET input stage
- Internal frequency compensation
- Latch up free operation
- High slew rate: 16 V/µs (typical)

Description

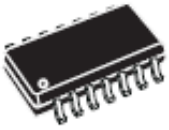
The TL084, TL084A, and TL084B are high-speed, JFET input, quad operational amplifiers incorporating well matched, high voltage JFET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

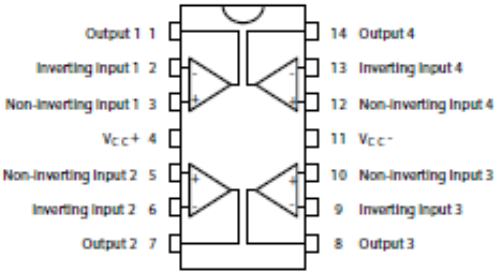
N
DIP14
(Plastic package)

D
TSSOP14
(Thin shrink small outline package)

D
SO-14
(Plastic micropackage)



Pin connections
(Top view)



4.2 Construction note

	P/N *LM2903YDT*	**P/N *LM2901YDT***	**P/N *TL084IYDT***	
Wafer/Die fab. information				
Wafer fab manufacturing location	ST Singapore	ST Singapore	ST Singapore	
Technology	Bipolar	Bipolar	JFet	
Die finishing back side	RAW SILICON	RAW SILICON	RAW SILICON	
Die size (microns)	950 x 870 µm	1370x1270	2480 x 1460	
Bond pad metallization layers	AlSiCu	AlSiCu	AlSiCu	
Passivation type	Nitride	Nitride	P-VAPOX/NITRIDE	
Wafer Testing (EWS) information				
Electrical testing manufacturing location	ST Singapore	ST Singapore	ST Singapore	
Tester	ASL1K	ASL1K	ASL1K	
Assembly information				
Assembly site	ST Bouskoura	ST Bouskoura	ST Bouskoura	
Package description	SO8	SO14	SO14	
Molding compound	EME G700KC	EME G700KC	EME G700KC	
Frame material	Cu	Cu	Cu	
Die attach process	Epoxy Glue	Epoxy Glue	Epoxy Glue	
Die attach material	8601S-25	8601S-25	8601S-25	
Wire bonding process	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding	
Wires bonding materials/diameters	Cu 1 mil	Cu 1 mil	Cu 1 mil	
Lead finishing process	electroplating	electroplating	electroplating	
Lead finishing/bump solder material	Matte tin	Matte tin	Matte tin	
Final testing information				
Testing location	ST Bouskoura	ST Bouskoura	ST Bouskoura	
Tester	ASL1K	ASL1K	ASL1K	

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	Bipolar/SO8	0393	CZ53005LR
2	Bipolar/SO14	0339	CZ52405FR
3	JFet / So14	0084	CZ53306W

5.2 Test plan and results summary

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS				Note
						Lot 1 0393	Lot 2 0339	Lot 3 0084		
HTB	N	JESD22 A-108	Tj = 150°C, BIAS		168 H	0/78	0/78			
					500 H	0/78	0/78			
					1000 H	78	0/78			
HTSL	N	JESD22 A-103	Ta = 150°C		168 H	6X0/77	3x0/77	77		(1)
					500 H	6X0/77	3x0/77	77		
					1000 H	6X77	3x0/77	77		
					2000H					
Package Oriented Tests										
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Over Reflow @ Tpeak=260°C 3 times		Final	PASS	PASS	PASS		
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C		96 H	6x0/77	3x0/77	77		(1)
TC	Y	JESD22 A-104	Ta = -65°C to 150°C		100 cy	6x0/77	3x0/77	77		(1)
					200 cy	6x0/77	3x0/77	77		
					500 cy	6x0/77	3x0/77	77		
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, BIAS		168 H		0/78			
					500 H		78			
					1000 H		78			
Other Tests										
ESD	N	AEC Q101-001, 002 and 005	CDM							
						3	3	3		
SD	N		After ageing 8h and 16h			X	X			

(1) Additional split lot to cover the whole assembly variability

For reference, below the reliability assessment made on Sumitomo G700K

	P/N LM324DT	P/N TSV632IDT	P/N TSx922IDT	P/N TSX3702IDT	P/N TSX393IDT	P/N TSX3702IDT	P/N LM358DT
Wafer/Die fab. information							
Wafer fab manufacturing location	AMJ9	Crolles	Agrate	Agrate	Agrate	Agrate	AMK6
Technology	Bipolar	HCMOS5LA	HVG8A	HVG8A	HVG8A	HVG8A	Bipolar
Process family	Bipolar	HCMOS5LA	HVG8A	HVG8A	HVG8A	HVG8A	Bipolar
Die finishing back side	Raw silicon	Raw silicon	Raw silicon	Raw silicon	Raw silicon	Raw silicon	Raw silicon
Die size	1430x 1360 µm	1020 x 1090 µm	1700x1400 µm	1018x1238 µm	1018x1238 µm	1018x1238 µm	1070x1010 µm
Bond pad metallization layers	AlSiCu	AlCu	AlCu	AlCu	AlCu	AlCu	AlSiCu
Passivation type	Nitride	PSG + NITRIDE + PIX	HDP/TEOS/SiN /Polyimide	HDP/TEOS/SiN /Polyimide	HDP/TEOS/Si N/Polyimide	HDP/TEOS/Si N/Polyimide	Nitride
Wafer Testing (EWS) information							
Electrical testing manufacturing location	ST Singapore	ST Singapore	ST Singapore	ST Singapore	ST Singapore	ST Singapore	ST Singapore
Tester	ASL1K	ASL1K	ASL1K	ASL1K	ASL1K	ASL1K	ASL1K
Assembly information							
Assembly site	Bouskoura	Bouskoura	Bouskoura	Bouskoura	Bouskoura	Bouskoura	Bouskoura
Package description	SO14	SO8	SO8	SO8	SO8	SO8	SO8
Molding compound	Sumitomo G700K	Sumitomo G700K	Sumitomo G700K	Sumitomo G700K	Sumitomo G700K	Sumitomo G700K	Sumitomo G700K
Frame material	Cu	Cu	Cu	Cu	Cu	Cu	Cu
Die attach process	Glue	Glue	Glue	Glue	Glue	Glue	Glue
Die attach material	Abkestick 8601-S25	Abkestick 8601-S25	Abkestick 8601-S25	Abkestick 8601-S25	Abkestick 8601-S25	Abkestick 8601-S25	Abkestick 8601-S25
Die pad size	75 x 75 µm²	75 x 75 µm²	75 x 75 µm²	75 x 75 µm²	75 x 75 µm²	75 x 75 µm²	75 x 75 µm²
Wire bonding process	Thermosonic Ball bonding	Thermosonic Ball bonding	Thermosonic Ball bonding	Thermosonic Ball bonding	Thermosonic Ball bonding	Thermosonic Ball bonding	Thermosonic Ball bonding
Wires bonding materials/diameters	Cu 1 mil	Cu 1 mil	Cu 1 mil	Cu 1 mil	Cu 1 mil	Cu 1 mil	Cu 1 mil
Lead finishing process	preplated	preplated	preplated	preplated	preplated	preplated	preplated
Lead finishing/bump solder material	NiPdAgAu	NiPdAgAu	NiPdAgAu	NiPdAgAu	NiPdAgAu	NiPdAgAu	NiPdAgAu
Final testing information							
Testing location	Bouskoura	Bouskoura	Bouskoura	Bouskoura	Bouskoura	Bouskoura	Bouskoura
Tester	ASL1K	ASL1K	ASL1K	ASL1K	ASL1K	ASL1K	ASL1K

Test	PC	Std ref.	Conditions	Steps	Lot 1	Lot 2	Lot 3	Lot 4	Lot 5	Lot 6	Lot 7	Note
Die Oriented Tests												
HTB	N	JESD22 A-108	Tj = 125°C, BIAS	168 H	0 / 78	0 / 78	0 / 78	0 / 78	0 / 78		0 / 78	
				500H	0 / 78	0 / 78	0 / 78		0 / 78	0 / 78	0 / 78	
				1000H	0 / 78	0 / 78	0 / 78		0 / 78		0 / 78	
HTSL	N	JESD22 A-103	Ta=150°C	168 H	0 / 78	0 / 78			0 / 78		0 / 76	
				500H	0 / 78	0 / 78			0 / 78		0 / 76	
				1000H	0 / 78	0 / 78			0 / 78		0 / 76	
Package Oriented Tests												
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Over Reflow @ Tpeak=260°C 3 times	Final	PASS	PASS	PASS	PASS	PASS	PASS	PASS	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C	96 H								
				168 H	0 / 78	0 / 78			0 / 80		0 / 116	
TC	Y	JESD22 A-104	Ta = -65°C to 150°C	100 cy							0 / 77	
				500 cy	0 / 78	0 / 78	0 / 78	0 / 80	0 / 78		0 / 77	
				1000 cy							0 / 77	
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, BIAS	168H	0 / 78	0 / 78			0 / 78		0 / 78	
				1000H	0 / 78	0 / 78			0 / 78		0 / 78	

	P/N TSH95IDT	P/N HCF4093BMTR	P/N TS393IDT	P/N TS912IDT	P/N TSV912IDT	P/N TS924IDT
Wafer/Die fab. information						
Wafer fab manufacturing location	AMK6	AMK6	AMK6	AMK6	UMC	AMK6
Technology	HF2CMOS	Metal Gate	HC1PA	HC1PA	HF5CMOS	HF2CMOS
Process family	HF2CMOS	Metal Gate	HC1PA	HC1PA	HF5CMOS	HF2CMOS
Die finishing back side	Raw silicon	Raw silicon	Raw silicon	Raw silicon	Raw silicon	Raw silicon
Die size	1990x2700 µm	1480x930 µm	1390x1010 µm	2630x1980 µm	1070x110 µm	1980x2450 µm
Bond pad metallization layers	AlSiCu	AlSi	AlSi	AlSi	AlCu	AlSiCu
Passivation type	P-VAPOX(SiO2) / NITRIDE (SiN)	P-VAPOX(SiO2) / NITRIDE (SiN)	P-VAPOX(SiO2) / NITRIDE (SiN)	P-VAPOX(SiO2) / NITRIDE (SiN)	P-VAPOX(SiO2) / NITRIDE (SiN)	P-VAPOX(SiO2) / NITRIDE (SiN)
Wafer Testing (EWS) information						
Electrical testing manufacturing location	ST Singapore	ST Singapore	ST Singapore	ST Singapore	ST Singapore	ST Singapore
Tester	ASL1K	ASL1K	ASL1K	ASL1K	ASL1K	ASL1K
Assembly information						
Assembly site	Bouskoura	Bouskoura	Bouskoura	Bouskoura	Bouskoura	Bouskoura
Package description	SO16	SO14	SO8	SO8	SO8	SO14
Molding compound	Sumitomo G700K	Sumitomo G700K	Sumitomo G700K	Sumitomo G700K	Sumitomo G700K	Sumitomo G700K
Frame material	Cu	Cu	Cu	Cu	Cu	Cu
Die attach process	Glue	Glue	Glue	Glue	Glue	Glue
Die attach material	Abkestick 8601-S25	Abkestick 8601-S25	Abkestick 8601-S25	Abkestick 8601-S25	Abkestick 8601-S25	Abkestick 8601-S25
Wire bonding process	Thermosonic Ball bonding	Thermosonic Ball bonding	Thermosonic Ball bonding	Thermosonic Ball bonding	Thermosonic Ball bonding	Thermosonic Ball bonding
Wires bonding materials/diameters	Cu 1 mil	Cu 1 mil	Cu 1 mil	Cu 1 mil	Cu 1 mil	Cu 1 mil
Lead finishing process	preplated	preplated	preplated	preplated	preplated	preplated
Lead finishing/bump solder material	NiPdAgAu	NiPdAgAu	NiPdAgAu	NiPdAgAu	NiPdAgAu	NiPdAgAu
Final testing information						
Testing location	Bouskoura	Bouskoura	Bouskoura	Bouskoura	Bouskoura	Bouskoura
Tester	ASL1K	ASL1K	ASL1K	ASL1K	ASL1K	ASL1K

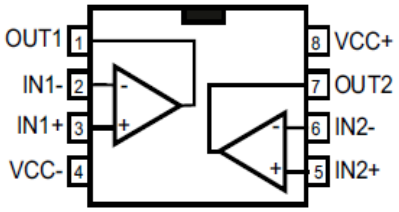
Test	PC	Std ref.	Conditions	Steps	Failure/SS Lot 1	Lot 2	Lot 3	Lot 4	Lot 5	Lot 6	Lot 7	Note
Die Oriented Tests												
HTB	N	JESD22 A-108	Tj = 125°C, BIAS	168 H	0 / 78	0 / 78	0 / 78	0 / 78	0 / 78		0 / 78	
				500H	0 / 78	0 / 78	0 / 78		0 / 78	0 / 78	0 / 78	
				1000H	0 / 78	0 / 78	0 / 78		0 / 78		0 / 78	
HTSL	N	JESD22 A-103	Ta=150°C	168 H	0 / 78	0 / 78			0 / 78		0 / 76	
				500H	0 / 78	0 / 78			0 / 78		0 / 76	
				1000H	0 / 78	0 / 78			0 / 78		0 / 76	
Package Oriented Tests												
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Over Reflow @ Tpeak=260°C 3 times	Final	PASS	PASS	PASS	PASS	PASS	PASS	PASS	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C	96 H								
				168 H	0 / 78	0 / 78			0 / 80		0 / 116	
TC	Y	JESD22 A-104	Ta = -65°C to 150°C	100 cy							0 / 77	
				500 cy	0 / 78	0 / 78	0 / 78	0 / 80	0 / 78		0 / 77	
				1000 cy							0 / 77	
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, BIAS	168H	0 / 78	0 / 78			0 / 78		0 / 78	
				1000H	0 / 78	0 / 78			0 / 78		0 / 78	

6 ANNEXES

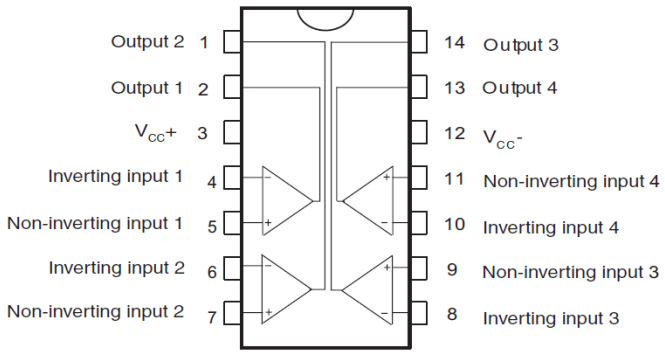
6.1 Device details

6.1.1 Pin connection

LM2903

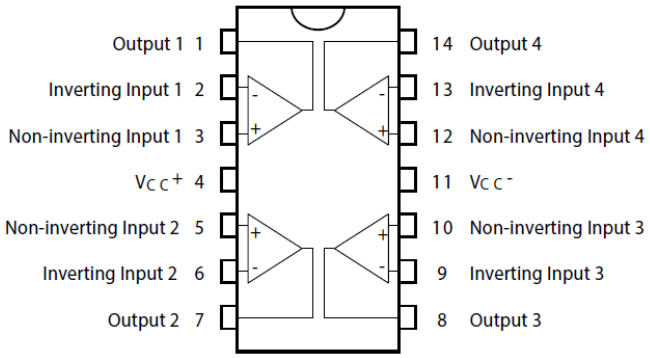


LM2901



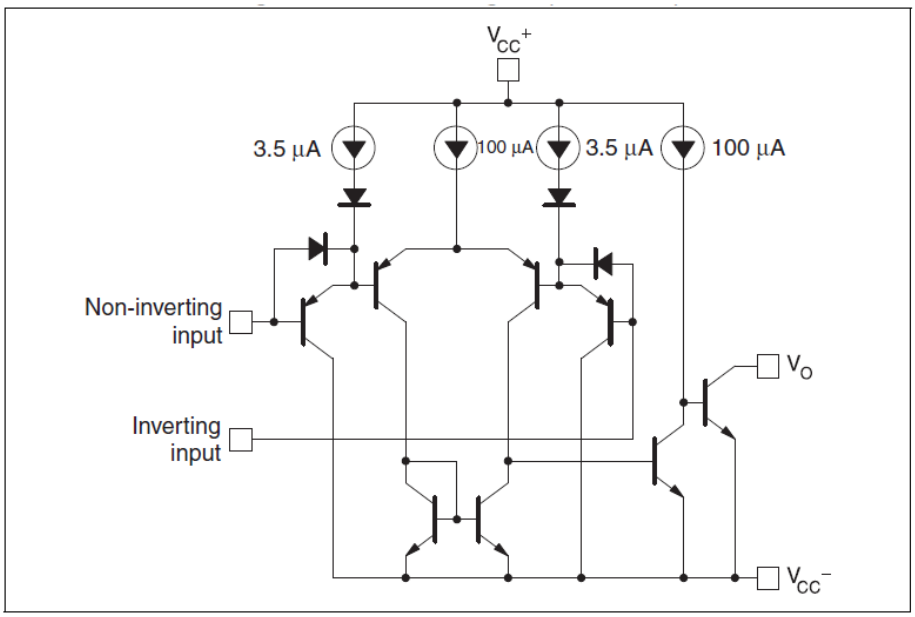
TL084

Pin connections
(Top view)

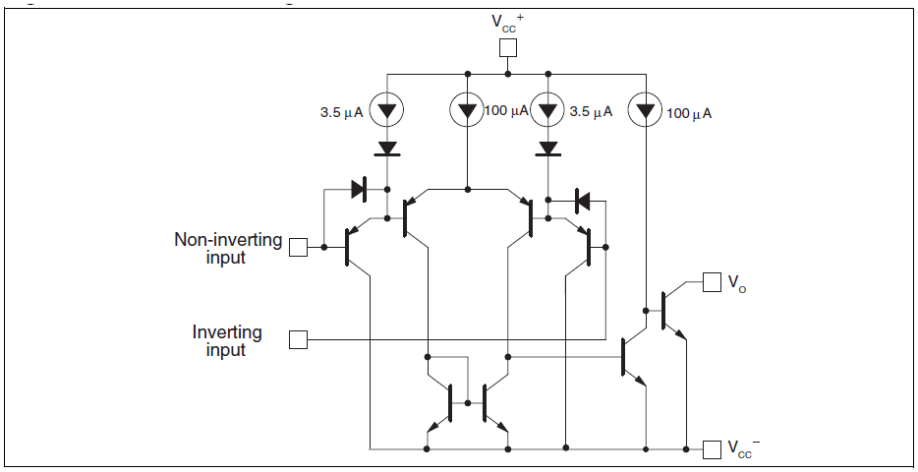


6.1.2 Block diagram

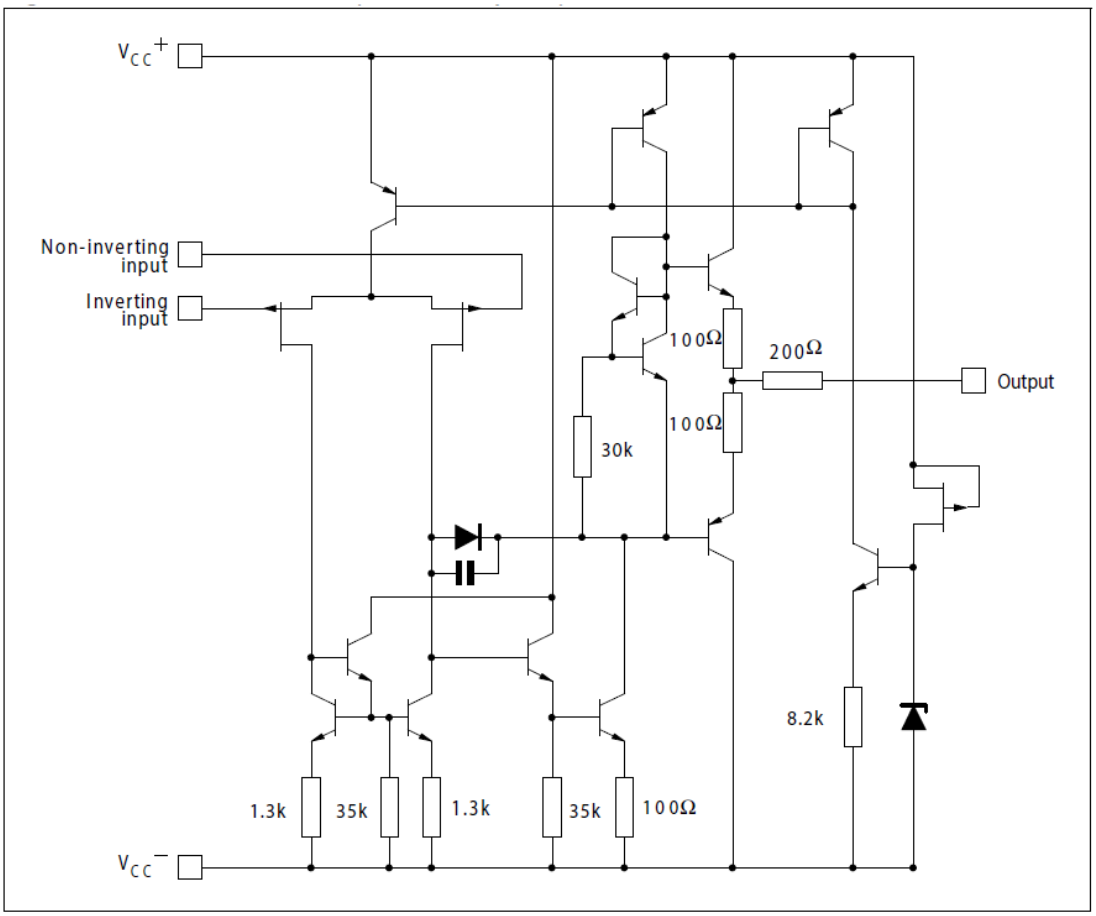
LM2903



LM2901



TL084


V_{CC}^+
Non-inverting input
Inverting input
100Ω
200Ω
Output
100Ω
30k
8.2k
1.3k
35k
1.3k
35k
100Ω
V_{CC}^-

6.2 Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operating Life **HTB** High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTRB High Temperature Reverse Bias **HTFB / HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: low power dissipation; max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
ELFR Early Life Failure Rate	The device is stressed in biased conditions at the max junction temperature.	To evaluate the defects inducing failure in early life.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.

Test name	Description	Purpose
TF / IOL Thermal Fatigue / Intermittent Operating Life	The device is submitted to cycled temperature excursions generated by power cycles (ON/OFF) at T ambient.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. CBM: Charged Device Model HBM: Human Body Model MM: Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
LU Latch-Up	The device is submitted to a direct current forced/sunk into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effect inducing latch-up.